CLAIMS:

1. A semiconductor device (10) comprising a plurality of layers, the semiconductor device (10) comprising:

- a substrate (20) having a first major surface,
- an inductive element (11) fabricated on the first major surface of the substrate (20), the inductive element (11) comprising at least one conductive line,
- a plurality of tilling structures in at least one layer,

wherein the plurality of tilling structures are electrically connected together and arranged in a geometrical pattern (14) so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element (11).

2. A semiconductor device (10) according to claim 1, the tilling structures being made from tilling structure material, wherein the plurality of tilling structures are arranged in a pattern so that the amount of tilling structure material in an area closer to the inductive element (11) is smaller than the amount of tilling structure material in an area farther away from the inductive element (11).

3. A semiconductor device (10) according to claim 1, wherein the tilling structures are located at different layers, tilling structures at each layer being arranged in a geometrical pattern (14) so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element (11).

4. A semiconductor device (10) according to claim 3, wherein the geometrical pattern (14) of tilling structures at two different layers is different in shape and/or orientation.

5. A semiconductor device (10) according to claim 3, wherein the tilling structures at different layers are electrically connected (13) to each other.

6. A semiconductor device (10) according to claim 1, wherein the tilling structures are connected to a DC potential.

7. A semiconductor device (10) according to claim 1, wherein the tilling structures are a plurality of slender elongate elements (12).

8. A semiconductor device (10) according to claim 1, wherein the tilling structures are a plurality of substantially triangular elements (71).

9. A semiconductor device (10) according to claim 7, wherein the elements (31) of the tilling structures are locally oriented perpendicular to the at least one conductive line of the inductive element (11).

10. A semiconductor device (10) according to claim 8, wherein the elements (31) of the tilling structures are locally oriented perpendicular to the at least one conductive line of the inductive element (11).

11. A semiconductor device (10) according to claim 1, furthermore comprising a ground shield (22) for shielding the inductive element (11) from a further layer.

12. A semiconductor device (10) according to claim 11, wherein the further layer is the substrate (20).

13. A semiconductor device (10) according to claim 10, furthermore comprising connection means (21) electrically connecting the plurality of tilling structures with the ground shield (22) without creating a conductive loop.

14. A semiconductor device (10) according to claim 1, wherein the tilling structures are formed in a region other than a region directly below the inductive element (11).

15. A semiconductor device (10) according to claim 1, furthermore provided with a further passive element.

16. A semiconductor device (10) according to claim 15, wherein the further passive element is a capacitive element (100).

17. A semiconductor device (10) according to claim 16, wherein the capacitive element (100) comprises two capacitor electrodes (101, 102), at least one of the capacitor electrodes being formed by a plurality of tilling structures.

18. A semiconductor device (10) according to claim 17, wherein a capacitor electrode formed by a plurality of tilling structures leads to a metal or polysilicon or active region density in the inductor vicinity respecting the design rules of advanced IC technologies.

19. A semiconductor device (10) according to claim 17, wherein one capacitor electrode of the capacitive element (100) is formed by the ground shield (111).

20. A semiconductor device (10) according to claim 15, wherein the integration of the capacitive element (100) with the inductive element (11) is optimized to respect the metal pattern density in advanced silicon technologies.

21. A semiconductor device (10) according to claim 15, wherein the distance between the capacitive element (100) and the inductive element (11) is large enough to avoid a dominant fringe coupling between them.

22. A method for providing an inductive element in a semiconductor device comprising a plurality of layers, the method comprising:

- providing a substrate having a first major surface,
- forming an inductive element above the first major surface of the substrate, the inductive element comprising at least one conductive line,
- providing a plurality of tilling structures in at least one layer,

wherein the plurality of tilling structures are electrically connected together and are arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element.